INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO FORM 1449

Atty. Docket No. 02885/85	Serial No. 10/791,501	
Applicant(s) Vorbach et al.		
Filing Date	Group Art Unit	
March 1, 2004	2116	

006 3		U. S. PATENT DOC	UMENTS			
AND S STATES	PATENT/ PUBLICATION NUMBER	PATENT/ PUBLICATION DATE	NAME	CLASS	SUB CLASS	FILING DATE
JKT	2,067,477	January 12, 1937	J.B. Cooper	1		
1	3,242,998	March 29, 1966	C.H. Gubbins	1		
	3,681,578	August 1, 1972	Stevens			
	3,757,608	September 11, 1973	Willner		-	
JKT	3,855,577	December 17, 1974	Vandierendonck			1
	4,480,857	February 6, 1986	Agrawal et al			
лкт	4,498,134	February 5, 1985	Hansen et al.	1	-	
UNI I	4,498,172	February 5, 1985	Bhavsar	1		<u> </u>
	4,566,102	January 21, 1986	Hefner			
	4,663,706	May 5, 1987	James et al.			1
	4,682,284	July 21, 1987	Schrofer		1	1
	4,720,780	January 19, 1988	Dolecek		1	1
	4,739,474	April 19, 1988	Holsztynski			/
	4,761,755	August 2, 1988	Ardini et al.			
	4,852,043	July 25, 1989	Guest		1	
	4,860,201	August 22, 1989	Miranker et al.		-\/	
	4,891,810	January 2, 1990	de Corlieu et al.			
	4,910,665	March 20, 1990	Mattheyses et al.		$-\sqrt{-}$	
	5,047,924	September 10, 1991	Matsubara et al.		- X -	
	5,065,308	November 12, 1999	Evans		/\	
•	5,072,178	December 10, 1991	Matsumoto		-/\	
	5,144,166	September 1, 1992	Camarota et al.		-/ \	
	5,193,202	March 9, 1993	Lee et al.		-/	
	5,203,005	April 13, 1993	Horst			
	5,274,593	December 28, 1993	Proebsting			/
	5,294,119	March 15, 1994	Vincent et al.		T - T	1
	5,301,284	April 5, 1994	Estes et al.		 	1
<u> </u>	5,347,639	September 13, 1994	Rechtschaffen et al.			1
	5,349,193	September 20, 1994	Mott et al.	1	·····	1
	5,353,432	October 4, 1994	Richek et al.			
	5,379,444	January 3, 1995	Mumme	 		
	5,410,723	April 25, 1995	Schmidt et al.	//		\
	5,425,036	June 13, 1995	Liu et al.	-		
	5,428,526	June 27, 1995	Flood et al.	1		
	5,465,375	November 7, 1995	Thepaut et al.	1		
JKT	5,475,856	December 12, 1995	Kogge	1		-

INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO FORM 1449

Atty. Docket No. 02885/85	Serial No. 10/791,501	
Applicant(s) Vorbach et al.		
Filing Date	Group Art Unit	
March 1 2004	l 2116	

FILING	SUB CLASS	CLASS	NAME	PATENT/ PUBLICATION DATE	PATENT/ PUBLICATION NUMBER	EXAMINER'S INITIALS
· · · · · · · · · · · · · · · · · · ·		1	Takano	June 25, 1996	5,530,873	JKT
			Bouvier et al.	June 25, 1996	5,530,946	•
			Halverson Jr. et al.	November 12, 1996	5,574,930	
			El Gamal Abbas et al.	February 4, 1997	5,600,265	
		1	Gilson	February 4, 1997	5,600,845	
1			Pitts	March 11, 1997	5,611,049	
1			Kromer	April 29, 1997	5,625,806	
		1	Selvidge et al.	July 15, 1997	5,649,176	
1		1	Steenstra et al.	July 15, 1997	5,649,179	
			Ogawara et al.	August 5, 1997	5,655,069	
			Matsumoto	August 12, 1997	5,657,330	
1			Mavity	October 7, 1997	5,675,743	
			Kuijsten	October 21, 1997	5,680,583	
			Vigil et al.	March 24, 1998	5,732,209	
			Barbier et al.	May 19, 1998	5,754,827	
			Tan	June 2, 1998	5,760,602	
			Jones	June 30, 1998	5,773,994	
	$\overline{}$		Barker et al.	August 11, 1998	5,794,059	
	X		Casselman	September 1, 1998	5,802,290	
			Cliff et al.	October 27, 1998	5,828,229	
			Shimomura et al.	December 8, 1998	5,848,238	
			Baxter	December 29, 1998	5,854,918	
			Norman	January 12, 1999	5,859,544	
			Сагт	February 2, 1999	5,865,239	
1	1.		Peters et al.	February 2, 1999	5,867,723	
	1		Hester et al.	March 16, 1999	5,884,075	
1			Williams et al.	March 23, 1999	5,887,162	
7		<u> </u>	Rodgers et al.	March 30, 1999	5,889,982	
			Eaton et al.	April 6, 1999	5,892,370	
		/	Davis III	May 4, 1999	5,901,279	
			Sindhu et al.	July 13, 1999	5,924,119	
1		_/	Baxter et al.	August 3, 1999	5,933,642	
+		-/-	Vorbach et al.	August 24, 1999	5,943,242	
-		-/	Cooke et al.	October 12, 1999	5,966,534	
		1	Cooke et al.	October 19, 1999	5,970,254	
	-	1	Gupta et al.	November 30, 1999	5,996,083	
		 	Vorbach et al.	February 1, 2000	6,021,490	JKT

INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO FORM 1449

Atty. Docket No. 02885/85	Serial No. 10/791,501	·
Applicant(s) Vorbach et al.		
Filing Date March 1, 2004	Group Art Unit	

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/ PUBLICATION DATE	NAME	CLASS	SUB CLASS	FILING DATE
JKT	6,023,564	February 8, 2000	Trimberger	1		
1	6,023,742	February 8, 2000	Ebeling et al.	1		7
	6,034,538	March 7, 2000	Abramovici			
	6,038,650	March 14, 2000	Vorbach et al.			
	6,038,656	March 14, 2000	Cummings et al.			
	6,047,115	April 4, 2000	Mohan et al.			
	6,049,222	April 11, 2000	Lawman			
	6,058,469	May 2, 2000	Baxter	1		
	6,081,903	June 27, 2000	Vorbach et al.	1		
	6,085,317	July 4, 2000	Smith			1
•	6,086,628	July 11, 2000	Dave et al.	<u> </u>	1	1
	6,088,795	July 11, 2000	Vorbach et al.		1	/
	6,092,174	July 18, 2000	Roussakov		\ /	
	6,105,105	August 15, 2000	Trimberger et al.		\	
	6,119,181	September 12, 2000	Vorbach et al.		\ /	
	6,125,408	September 26, 2000	McGee et al.		. \/	
	6,172,520	January 9, 2001	Lawman et al.		Y	
	6,173,434	January 9, 2001	Wirthlin et al.		Λ	
	6,202,182	March 13, 2001	Abramovici et al.		/\	
	6,219,833	April 17, 2001	Solomon et al.			
	6,230,307	May 8, 2001	Davis et al.		/	
	6,243,808	June 5, 2001	Wang			
	6,260,179	July 10, 2001	Ohsawa et al.			1
	6,263,430	July 17, 2001	Trimberger et al.			
	6,279,077	August 21, 2001	Nasserbakht et al.		1	
	6,282,627	August 28, 2001	Wong et al.			
	6,288,566	September 11, 2001	Hanrahan et al.			
	6,298,472	October 2, 2001	Phillips et al.			1
	6,311,200	October 30, 2001	Hanrahan et al.	/		
	6,321,366	November 20, 2001	Tseng et al.	. /		
	6,321,373	November 20, 2001	Ekanadham et al.		· · · · · · · · · · · · · · · · · · ·	
	6,338,106	January 8, 2002	Vorbach et al.			1
	6,341,318	January 22, 2002	Dakhil	1		1
	6,347,346	February 12, 2002	Taylor	1		1
JKT	6,349,346	February 19, 2002	Hanrahan et al.	1		1

. INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO FORM 1449

Atty. Docket No. 02885/85	Serial No. 10/791,501	
Applicant(s) Vorbach et al.		
Filing Date March 1, 2004	Group Art Unit	

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/ PUBLICATION DATE	NAME	CLASS	SUB CLASS	FILING DATE
JKT	6,370,596	April 9, 2002	Dakhil			
	6,378,068	April 23, 2002	Foster et al.	 		
	6,389,379	May 14, 2002	Lin et al.	\vdash		
	6,389,579	May 14, 2002	Phillips et al.			
· -	6,392,912	May 21, 2002	Hanrahan et al.			
	6,405,299	June 11, 2002	Vorbach et al.	 		
	6,421,817	July 16, 2002	Mohan et al.	1		
	6,435,054	October 10, 2000	Nguyen	1		
	6,425,068	July 23, 2002	Vorbach et al.	1		
	6,434,695	August 13, 2002	Esfanahi et al.		\	1
	6,457,116	September 24, 2002	Mirsky et al.	<u> </u>	\	\ <i>1</i>
	6,477,643	November 5, 2002	Vorbach et al.		1	//
	6,480,937	November 12, 2002	Vorbach et al.	,	\	/
	6,480,954	November 12, 2002	Trimberger et al.			
	6,513,077	January 28, 2003	Vorbach et al.		\ /	-
	6,519,674	February 11, 2003	Lam et al.		. \ /	
	6,526,520	February 25, 2003	Vorbach et al.		\ \ /	
	6,538,468	March 25, 2003	Moore		V	<u> </u>
	6,539,477	March 25, 2003	Seawright		X	
	6,542,844	April 1, 2003	Hanna		/\	
	6,542,998	April 1, 2003	Vorbach et al.		/\	
	6,571,381	May 27, 2003	Vorbach et al.		/ \	
	6,587,939	July 1, 2003	Takano		/	
	6,657,457	December 2, 2003	Hanrahan et al.			
	6,697,979	February 24, 2003	Vorbach et al.		:	1
	6,687,788	February 3, 2004	Vorbach et al.		1	1
	6,697,979	February 24, 2003	Vorbach et al.		1	
	6,704,816	March 9, 2004	Burke			1
	6,717,436	April 6, 2004	Kress et al.			
	6,728,871	April 27, 2004	Vorbach et al.	1		
	6,757,847	June 29, 2004	Farkash et al.	<i> </i>		1
	6,785,826	August 31, 2004	Durham et al.	1		1-1
	2001/0010074	July 6, 2001	Nishihara et al.	1		
	2002/0038414	March 28, 2002	Taylor et al.			1
	2002/0045952	April 18, 2002	Blemel	1		T 1
1	2002/0143505	October 3, 2002	Drusinsky	1		
JKT	2002/0144229	October 3, 2002	Hanrahan	1		

. INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO FORM 1449

Atty. Docket No. Serial No. 10/791,501		
Applicant(s) Vorbach et al.		
Filing Date	Group Art Unit	

EXAMINER'S INITIALS	PATENT/ PUBLICATION	PATENT/ PUBLICATION	NAME	CLASS	SUB CLASS	FILING DATE
INTIALS	NUMBER	DATE			CLASS	
JKT	2002/0165886	November 7, 2002	Lam	\		
	2003/0123579	July 3, 2003	Safavi et al.			/
	2003/0014743	January 16, 2003	Cooke et al.			
	2003/0046607	March 6, 2003	Vorbach			
	2003/0052711	March 20, 2003	Taylor et al.			
	2003/0055861	March 20, 2003	Lai et al.		1	
	2003/0056085	March 2, 2003	Vorbach			
	2003/0056091	March 20, 2003	Greenberg		$\overline{}$	
	2003/0056202	March 20, 2003	Vorbach			
	2003/0093662	May 15, 2003	Vorbach et al.			
	2003/0097513	May 22, 2003	Vorbach et al.			
	. 2003/0135686	July 17, 2003	Vorbach et al.		/	
	2003/0192032	October 9, 2003	Andrade et al.		/	
	2004/0015899	January 22, 2004	May et al.			
1	2004/0025005	February 5, 2004	Vorbach et al.		•	
JKT	2004/0168099	August 26, 2004	Vorbach et al		•	

FOREIGN PATENT DOCUMENTS

 $\frac{Abstract +}{Abstract} = English Abstract plus corresponding applications in patent family.$ Ab = English Abstract

EXAMINER'S		DATE	COUNTRY	CLASS	SUB-CLASS	TRANSL	ATION
INITIALS	NUMBER				:	YES	NO
JKT	0 208 457	January 14, 1987	EPO	\	/		
1	0 428 327	May 22, 1991	EPO				
	0 477 809	April 1, 1992	EPO				
	0 485 690	May 20, 1992	EPO				
	0 497 029	August 5, 1992	EPO				
	0 628 917	December 14, 1994	EPO				
	0 686 915	December 13, 1995	EPO	1			
	0 726 532	August 14, 1996	EPO		X		
	0 835 685	October 2, 1996	EPO	/			
	0 926 594	June 30, 1999	EPO				
	1 102 674	May 30, 2001	EPO			Ab	
	1 146 432	October 17, 2001	EPO			Ab	
	8-44581	February 16, 1996	Japan			Abstract +	
	7-154242	June 16, 1995	Japan			Abstract +	
JKT	58-58672	April 7, 1983	Japan			Abstract +	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO FORM 1449

Atty. Docket No. 02885/85	Serial No. 10/791,501		
Applicant(s) Vorbach et al.			
Filing Date March 1, 2004	Group Art Unit 2116		

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSI	LATION
INITIALS	NOWIBER					YES	NO
JKT	2-226423	September 10, 1990	Japan	1	1	Abstract +	
1	5-276007	October 22, 1993	Japan	1	1	Abstract +	
	8-250685	September 27, 1996	Japan	1		Abstract +	
	2-130023	May 18, 1990	Japan	1		Abstract +	
	2 752 466	February 20, 1998	France			Ab	
	38 55 673	November 20, 1996	Germany		1	Ab	
	42 21 278	January 5, 1994	Germany			Ab	
	100 28 397	December 20, 2001	Germany			Ab	
	100 36 627	February 14, 2002	Germany			Abstract +	
	101 29 237	April 18, 2002	Germany			Abstract +	
	102 04 044	August 14, 2003	Germany			Abstract +	
<u> </u>	197 04 044	August 13, 1998	Germany			Ab	
*****	197 04 742	September 24, 1998	Germany		1	Ab	
	198 07 872	August 26, 1999	Germany		 	Ab	
	198 61 088	February 10, 2000	Germany		 	Ab	
	WO94/06077	March 17, 1994	WIPO			Ab	
	WO98/26356	June 18, 1998	WIPO	1		Ab	
	WO98/28697	July 2, 1998	WIPO		1	Ab	
	WO98/29952	July 9, 1998	WIPO		/	Ab	
	WO98/31102	July 16, 1998	WIPO		\	Ab	
	WO98/35299	August 13, 1998	WIPO		1	Ab	
-	WO99/00731	January 7, 1999	WIPO	. 1			
	WO99/00739	January 7, 1999	WIPO		1		
	WO99/12111	March 11, 1999	WIPO				
	WO99/32975	July 1, 1999	WIPO		1	Ab	
	WO99/40522	August 12, 1999	WIPO	1			
	WO99/44147	September 2, 1999	WIPO			Ab	
	WO99/44120	September 2, 1999	WIPO		1	Ab	
	WO00/17771	March 30, 2000	WIPO	- -	<u> </u>	Ab	
	WO00/77652	December 21, 2000	WIPO		<u> </u>	Ab	
	WO00/38087	June 29, 2000	WIPO		1		
	WO01/55917	August 2, 2001	WIPO	<i> </i>			
	WO02/13000	February 14, 2002	WIPO	-		Ab	
	WO02/21010	March 14, 2002	WIPO			Ab	
	WO02/29600	April 11, 2002	WIPO			Ab	
	WO02/071248	September 12, 2002	WIPO	1	1	Ab	
	WO02/071249	September 12, 2002	WIPO	1			
JKT	WO02/103532	December 27, 2002	WIPO	 	-	Ab	

Atty. Docket No. Serial No. INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO FORM 1449 Atty. Docket No. Serial No. 10/791,501 Applicant(s) Vorbach et al. Filing Date March 1, 2004 Group Art Unit 2116

EXAMINER'S	DOCUMENT	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSI	LATION
INITIALS	NUMBER					YES	NO
JKT	WO03/017095	February 27, 2003	WIPO				
1	WO03/023616	March 30, 2003	WIPO			Ab	
	WO03/025781	March 27, 2003	WIPO			Ab	
	WO03/032975	April 24, 2003	WIPO				
JKT	WO03/036507	May 1, 2003	WIPO			Ab	

OTHER DOCUMENTS

** = referenced cited in previous IDS and re-cited to correct error in citation.

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.				
JKT	Ade et al., "Minimum Memory Buffers in DSP Applications," Electronics Letters, vol. 30, No. 6, March 17, 1994, pp. 469-471				
	Alippi, et al., "Determining the Optimum Extended Instruction Set Architecture for Application Specific Reconfigurable VLIW CPUs, IEEE., 2001, pp. 50-56				
	Arabi et al., "PLD Integrates Dedicated High-speed Data Buffering, Complex State Machine, and Fast Decode Array," conference record on WESCON '93, Sep. 28, 1993, pp. 432-436				
	Athanas, "A Functional Reconfigurable Architechture and Compiler for Adoptive Computing,", IEEE, pages 49-55.				
	Athanas, et al., "An Adaptive Hardware Machine Architecture and Compiler for Dynamic Processor Reconfiguration", IEEE, Laboratory for Engineering Man/Machine Systems Division of Engineering, Box D, Brown University Providence, Rhode Island, 1991, pages 397-400				
	Baumgarte, et al., PACT XPP "A Self-reconfigurable Data Processing Architecture," PACT Info. GMBH, Munchen Germany 2001, 7 pages				
	Beck et al., "From control flow to data flow," TR 89-1050, October 1989, Dept. of Computer Science, Cornell University, Ithaca, NY, pp. 1-25.				
	Becker, et al., "Parallelization in Co-compilation for Configurable Accelerators - a Host/accelerator Partitioning Compilation Method," proceedings of Asia and South Pacific Design Automation Conference, Yokohama, Japan, February 10-13, 1998, 11 pages.				
	Cadambi et al., "Managing Pipeline-reconfigurable FPGAs," ACM, 1998, pp. 55-64				
	Callahan, et al. "The Garp Architerchture and C Copiler," Computer, April 2000, pages 62-69.				
	Cardoso, "Compilation of Java TM Algorithms onto Reconfigurable Computing Systems with Exploitation of Operation- Level Parallelism," Ph.D. Thesis, Universidade Tecnica de Lisboa (UTL), Lisbon, Portugal October 2000 (Table of Contents and English Abstract only)				
	Diniz, et al., "Automatic Synthesis of Data Storage and Control Structures for FPGA-based Computing Engines", 2000 IEEE, pages 91-100.				
	Donandt, "Improving Response Time of Programmable Logic Controllers by Use of a Boolean Coprocessor", AEG Research Institute Berlin, IEEE, 1989, pages 4-167 - 4-169.				
	Dutt, et al., "If Software is King for Systems-on-Silicon, What's New in Compiler?, IEEE., 1997, pp. 322-325				
	Ferrante, et al., "The Program Dependence Graph and its Use in Optimization ACM Transactions on Programming Languages and Systems," July 1987, USA, [online] Bd. 9, Nr., 3, pages 319-349, XP002156651 ISSN: 0164-0935 ACN Digital Library				
	Fineberg, et al., "Experimental Analysis of a Mixed-Mode Parallel Architecture Using Bitonic Sequence Sorting", Vol. 11. No. 3, March 1991, pages 239-251				
JKT	Fornaciari, et al., System-level power evaluation metrics, 1997 Proceedings of the 2nd Annual IEEE International Conference on Innovative Systems in Silicon, New York, NY, October 1997, pp. 323-330.				

INFORMATION DISCLOSURE	Atty. Docket No. 02885/85	Serial No. 10/791,501	
STATEMENT BY APPLICANT PTO FORM 1449	Applicant(s) Vorbach et al.		
	Filing Date March 1, 2004	Group Art Unit 2116	

XAMINER'S	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.				
JKT	Gokhale, et al., "Automatic Allocation of Arrays to Memories in FPGA processors with Multiple Memory Banks", Field-Programmable Custom Computing Machines, 1999, IEEE, pages 63-67				
	Hammes, et al., "Cameron: High Level Language Compilation for Reconfigurable Systems," Department of Computer Science, Colorado State University, Conference on Parallel Architectures and Compilation Techniques, October 12-16, 1999, 9 pages.				
	Hauck, "The Roles of FPGA's in Reprogrammable Systems," IEEE, April 1998, pp. 615-638				
	Hauser, et al., "Garp: A MIPS Processor with a Reconfigurable Coprocessor", University of California, Berkeley, IEEE 1997, pages 24-33.				
	Hedge, "3D WASP Devices for On-line Signal and Data Processing, 1994, International Conference on Wafer Scale Integration, pages 11-21.				
:	Hwang, et al., "Min-cut Replication in Partitioned Networks" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, [online] Bd. 14, Nr. 1, January 1995, pages 96-106, (XP00053228 USA ISSN: 0278-0070 IEEE Xplore)				
	Iseli, et al. "A C++ Compiler for FPGA Custom Execution Units Synthesis," IEEE. 1995, pp. 173-179.				
	Isshiki, et al., "Bit-Serial Pipeline Synthesis for Multi-FPGA Systems with C++ Design Capture," 1996 IEEE, pp. 38-4				
	Jacob, et al., "Memory Interfacing and Instruction Specification for Reconfigurable Processors", ACM 1999, pages 145				
	Jantsch, et al., "A Case Study on Hardware/software Partitioning," Royal Institute of Technology, Kista, Sweden, April 10, 1994 IEEE, pp. 111-118				
	Koch, et al, "Practical Experiences with the SPARXIL Co-Processor", 1998, IEEE, pages 394 - 398				
	Kung,, "Deadlock Avoidance for Systolic Communication", 1988 Conference Proceedings of 15th Annual International Symposium on Computer Architecture, May 30, 1988, pp. 252-260				
	Ling et al., "WASMII: An MPLD with Data-Driven Control on a Virtual Hardware," Journal of Supercomputing, Kluwer Academic Publishers, Dordrecht, Netherlands, 1995, pp. 253-276.				
	Ling et al., "WASMII: A Multifunction Programmable Logic Device (MPLD) with Data Driven Control," The Transactions of the Institute of Electronics, Information and Communication Engineers, 25 April 1994, Vol. J77-D-1, Nr. 4, pp. 309-317. [This references is in Chinese, but should be comparable in content to the Ling et al. reference above]				
	Lizy, J., et al., "A Dynamically Reconfigurable Interconnect for Array Processors", Vol. 6, No. 1, March 1998, IEEE, pages 150-157				
	Miller, et al., "High-Speed FIFOs Contend with Widely Differing Data Rates: Dual-port RAM Buffer and Dual-pointer System Provide Rapid, High-density Data Storage and Reduce Overhead", Computer Design, September 1, 1985, pages 83-86.				
JKT	Mirsky, "MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources," Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, 1996, PP. 157-166.				
	"Myers, C., "Advances in Computer Architecture," Wiley-Interscience Publication, 2 nd Ed., John Wiley & Sons, Inc., 1978, pp. 463-494.				
JKT	Nilsson, et al., "The Scalable Tree Protocol - A Cache Coherence Approaches for Large-Scale Multiprocessors" IEEE, pp. 498-506 December 1992				
	Schmit, et al., Hidden Markov Modeling and Fuzzy Controllers in FPGAs, FPGAs for Custom Computing Machines, 1995; Proceedings, IEEE Symposium on Napa Valley, CA, April 1995, pp. 214-221.				
	Shirazi, et al., "Quantitative analysis of floating point arithmetic on FPGA based custom computing machines, IEEE Symposium on FPGAs for Custom Computing Machines," IEEE Computer Society Press, April 19-21, 1993, pp. 390-393.				
JKT	Siemers, "Rechenfabrik Ansaetze Fuer Extrem Parallele Prozessoren," Verlag Heinze Heise GmbH., Hannover, DE No 15, July 16, 2001, pages 170-179				

INFORMATION DISCLOSURE	Atty. Docket No. 02885/85	Serial No. 10/791,501	
STATEMENT BY APPLICANT PTO FORM 1449	Applicant(s) Vorbach et al.		
	Filing Date	Group Art Unit	

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.			
JKT Simunic, et al., Source Code Optimization and Profiling of Energy Co the 13th International Symposium on System Synthesis, September 2				
·	Tau, et al., "A First Generation DPGA Implementation," FPD'95, pp. 138-143			
	Tenca, et al., "A Variable Long-Precision Arithmetic Unit Design for Reconfigurable Coprocessor Architectures", University of California, Los Angeles, 1998, pages 216 - 225.			
	The XPP White Paper, Release 2.1, PACT - A Technical Perspective, March 2	7, 2002, pages 1-27.		
	TMS320C54X DSP: Volume 1: CPU and Peripherals, Texas Instruments, 1990	5, pp. 6-26 to 6-49		
	TMS320C54x DSP: Volume 2: Mnemonic Instruction Set, Texas Instruments, 1996, p. i-xi; 1-1 to 1-11; 2-1 to 2-21; 3 to 3-72; 4-1 to 4-203; A-1 to A-3; B-1 to B-7; -1 to C-5; D-1 to D-10, and Index.			
	Villasensor, et al., "Express Letters Video Communications Using Rapidly Reconfigurable Hardware," IEEE Transactions on Circuits and Systems for Video Technology, IEEE, Inc. NY, December 1995, pp. 565-567.			
	Wada, et al., "A Performance Evaluation of Tree-based Coherent Distributed Shared Memory" Proceedings of the Pacific RIM Conference on Communications, Comput and Signal Processing, Victoria, May 19-21, 1993, pp. 390-393.			
	Weinhardt, et al., "Pipeline Vectorization," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 2, February 2001, pp. 234-248.			
	Weinhardt, et al., "Pipeline Vectorization for Reconfigurable Systems", 1999, IEEE, pages 52-60			
	Wittig et al., "OneChip: An FPGA Processor with Reconfigurable Logic" IEEE, 1996 pp. 126-135			
	Wu et al., "A New Cache Directory Scheme", IEEE, pp 466-472, June 1996			
	Xu et al., "Parallel QR Factorization on a Block Data Flow Architecture" Conference Proceeding Article, March 1, 1992, pages 332-336 XPO10255276, PAGE 333, Abstract 2.2, 2.3, 2.4 - page 334			
	XLINX, "Logic Cell Array Families: XC4000, XC4000A and XC4000H", product description, pages 2-7 to 2-15, Additional XC3000, XC31000 and XC3100A Data, pp. 2-7, 2-9, 2-14, 2-15, 8-16, and 9-14.			
	Ye, Z.A. et al., "A Compiler for a Processor With A Reconfigurable Functional Unit," FPGA 2000 ACM/SIGNA International Symposium on Field Programmable Gate Arrays, Monterey, CA Feb. 9-11, 2000, pp. 95-100.			
JKT	JKT Zhang, N. et al., Architectural Evaluation of Flexible Digital Signal Processing for Wireless Receivers, Signals, Systems and Computers, 2000; Conference Record of the Thirty-Fourth Asilomar Conference, Bd.1, 29 October 2000, pp. 78-83.			
EXAMINER	/James K. Trujillo/	02/23/2007		
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.				